BASIC ELECTRONICS ENGINEERING
(RBL1B002)

MODULE-1

BJT DC BIASING

- 4 types of biasing circuits are there.
  - Fixed Bias Circuit
  - Emitter Stabilized Bias Circuit
  - Voltage Divider Bias Circuit
  - DC bias with voltage feedback

<u>NOTE:</u>

1. $I_E = I_B + I_C$

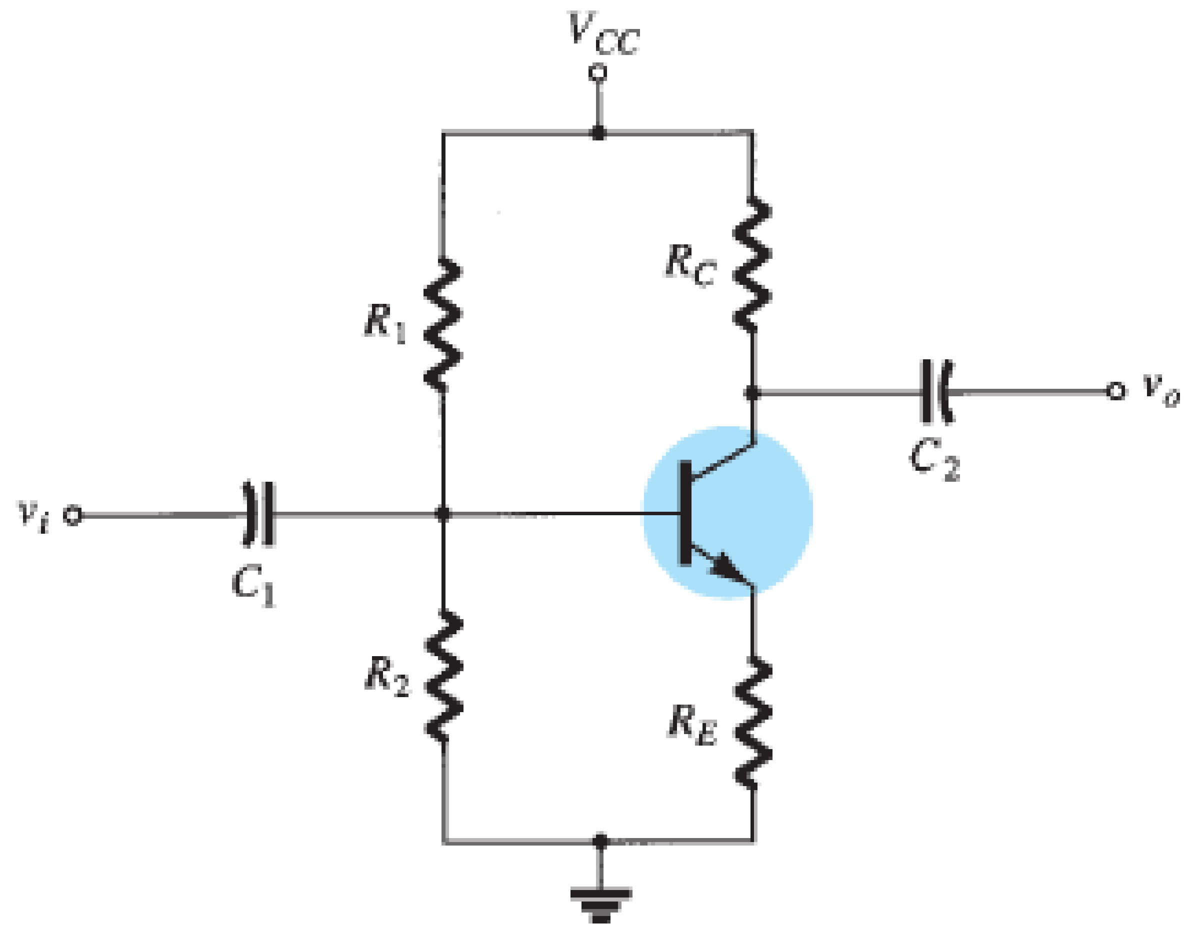
2. $\beta = \frac{I_C}{I_B}$

3. $I_E \approx I_C$

4. $V_{BE} = \begin{cases} 0.7\ for\ Si \\ 0.3\ for\ Ge \end{cases}$

5. $V_{XY} = V_X - V_Y$

Voltage Divider Bias Circuit



Voltage Divider Bias Circuit

- In the previous bias configurations, the bias current I_{CQ} and voltage V_{CEQ} at Q point were a function of the current gain (β) of the transistor.
- Since β is temperature sensitive it is desirable to develop a bias circuit that is independent of transistor β or less dependent on β .
- The Voltage divider bias configuration provides such type of network.
- If the circuit parameters are properly chosen the resulting levels of I_{CQ} and V_{CEQ} can be almost totally independent of β.

Voltage Divider Bias Circuit

There are two methods that can be applied to analyse the voltage divider configuration.

1) Exact Analysis
2) Approximate Analysis

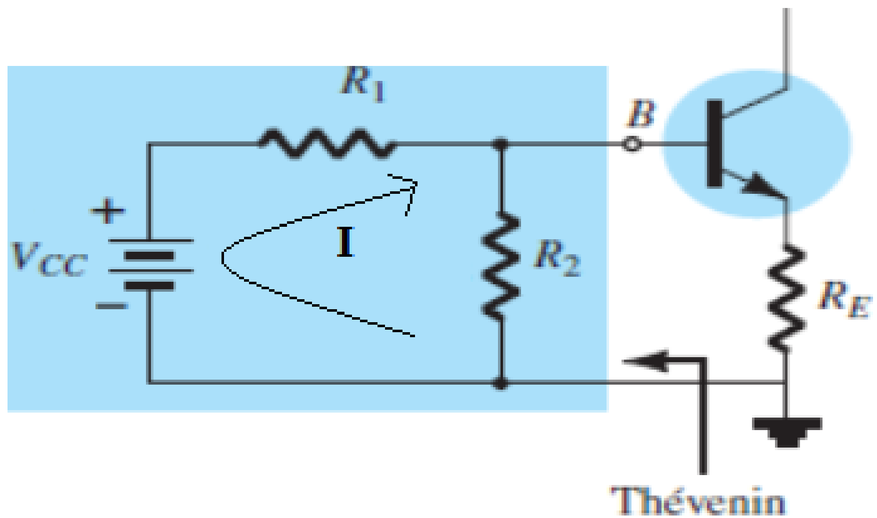
The exact analysis can be applied to any voltage divider configuration.

But the approximate method can be applied only if some specific conditions are satisfied.

Voltage Divider Bias Circuit

EXACT Analysis:

The BE junction of the voltage divider bias circuit can be redrawn as



Voltage Divider Bias Circuit

Assuming the current I, by KVL

$V_{CC} - IR_1 - IR_2 = 0$

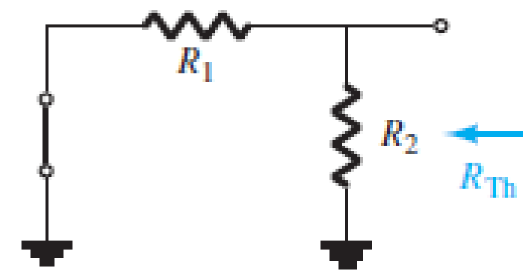
$\Rightarrow I = \frac{V_{CC}}{R_1 + R_2}$

Hence the voltage across R2 i.e. thevenin's voltage is given by

$$E_{Th} = I \times R_2 = \frac{R_2 V_{CC}}{R_1 + R_2}$$

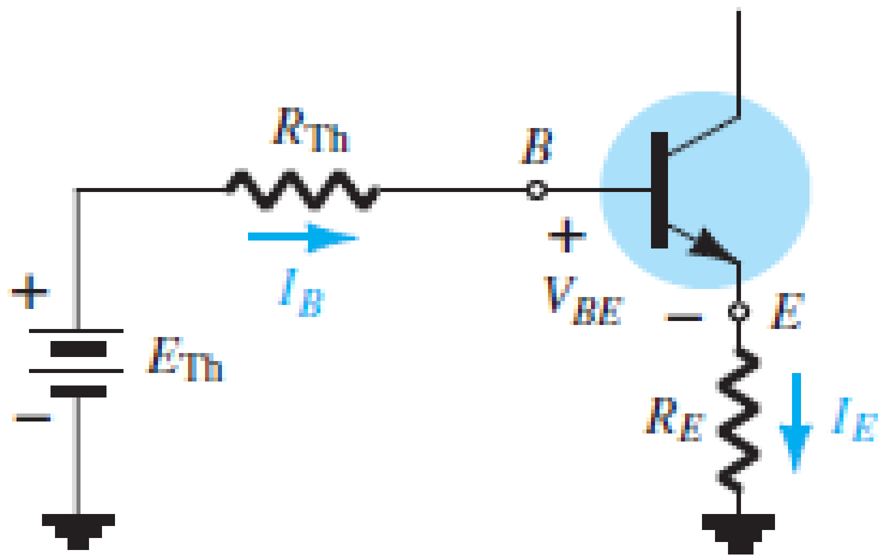
And the thevenin's resistance is given by

$$R_{TH} = R_1\ R_2 = \frac{R_1 R_2}{R_1 + R_2}$$



Voltage Divider Bias Circuit

Hence the BE loop can be redrawn as



Voltage Divider Bias Circuit

Now by KVL in this BE loop, we have

$E_{TH} – I_B.R_{TH} – V_{BE} – I_E .R_E = 0$

$=> E_{TH} – V_{BE} – I_B R_{TH} – (\beta +1) I_{B.} R_E= 0$

$\Rightarrow E_{TH} – V_{BE} = I_B [R_{TH} + (\beta +1) R_E]$

$$\Rightarrow I_B = \frac{E_{TH}-V_{BE}}{R_{TH}+(\beta+1)R_E}$$

Now $I_C = \beta I_B$

Voltage Divider Bias Circuit

Now by KVL in this CE loop, we have

$V_{CC} – I_C R_C – V_{CE} – I_E R_E = 0$

Substituting $I_E \approx I_C$

$V_{CE} = V_{CC} – I_C R_C – I_C R_E$

=> $V_{CE} = V_{CC} – I_C (R_C + R_E)$

$V_{CE} = V_C – V_E$ & $V_E = I_E R_E$

$V_C = V_{CE} + V_E$

$V_B = V_{BE} + V_E$

Load Line Analysis – Voltage Divider Bias Circuit

The CE loop of the fixed bias circuit:

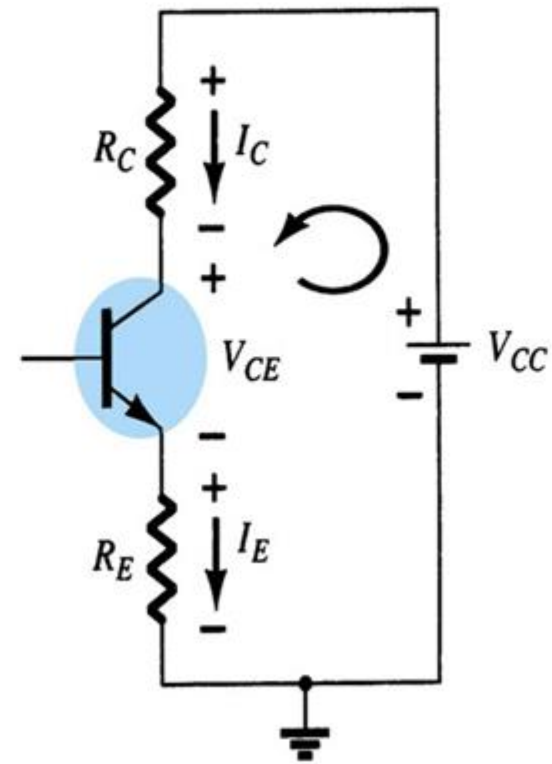
By KVL:

$V_{CC} – I_C R_C – V_{CE} – I_E R_E = 0$

$\Rightarrow V_{CE} = V_{CC} – I_C (R_C + R_E)$

Let $I_C = 0$, So $V_{CE} = V_{CC}$

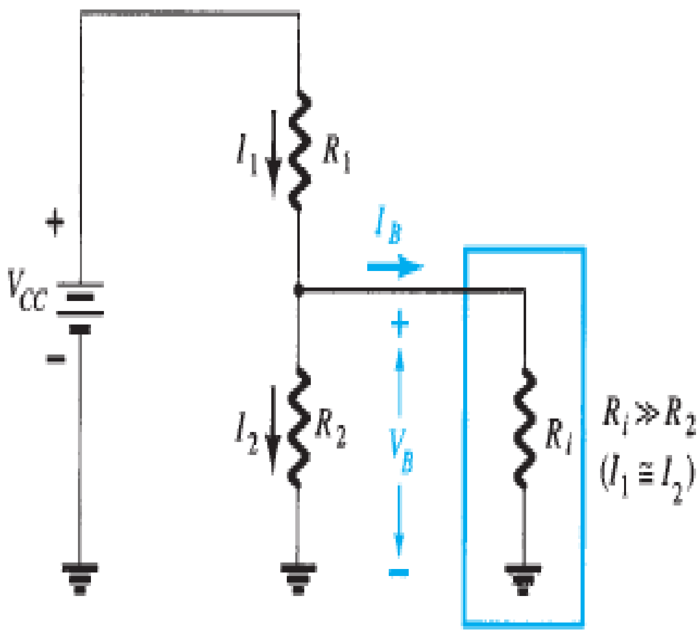
Again, let $V_{CE} = 0$, So $I_C = V_{CC} / (R_C + R_E)$



Voltage Divider Bias Circuit

Approximate Analysis: $(\beta R_E \geq 10 R_2)$

The input section of the voltage divider configuration can be represented by



R_i is the equivalent resistance between base & ground for the transistor with emitter resistance R_E.

Assuming $R_i >> R_E$, we have $I_B = 0$. Hence $I_1 = I_2$ and R_1 & R_2 can be considered as series.

Voltage Divider Bias Circuit

So by voltage division rule, the voltage across R_2 which is the base voltage is given by

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Since R_i =(β+1) $R_E \approx \beta R_E$, the condition for this analysis can be chosen as $\beta R_E \geq 10 R_2$.

Now $V_E = V_B - V_{BE}$

The emitter current can be determined as,

$$I_E = \frac{V_E}{R_E}$$

and, $I_C \approx I_E$

Voltage Divider Bias Circuit

Now by applying KVL in CE loop

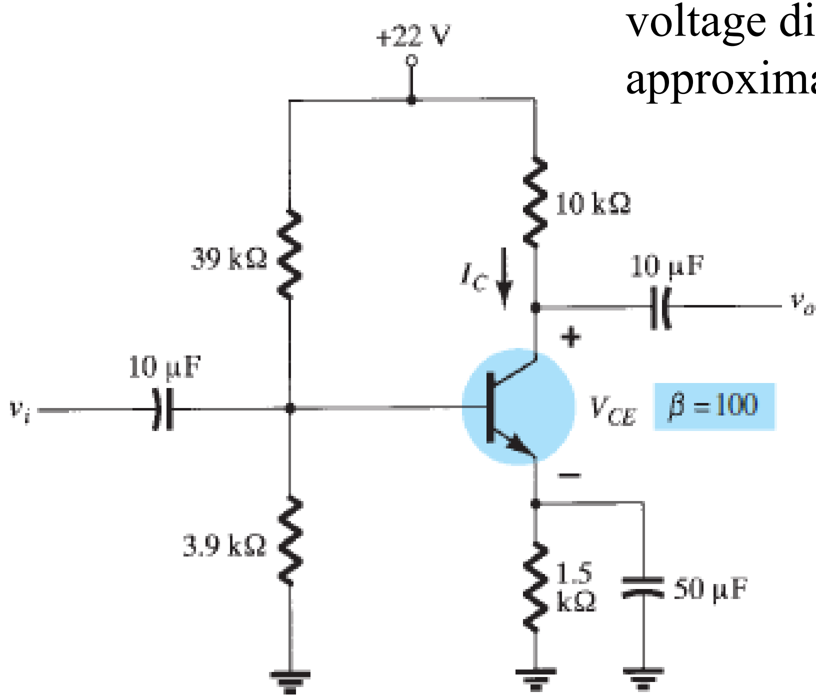
$$V_{CE} = V_{CC} - I_C\,(R_C + R_E)$$

PRACTICE

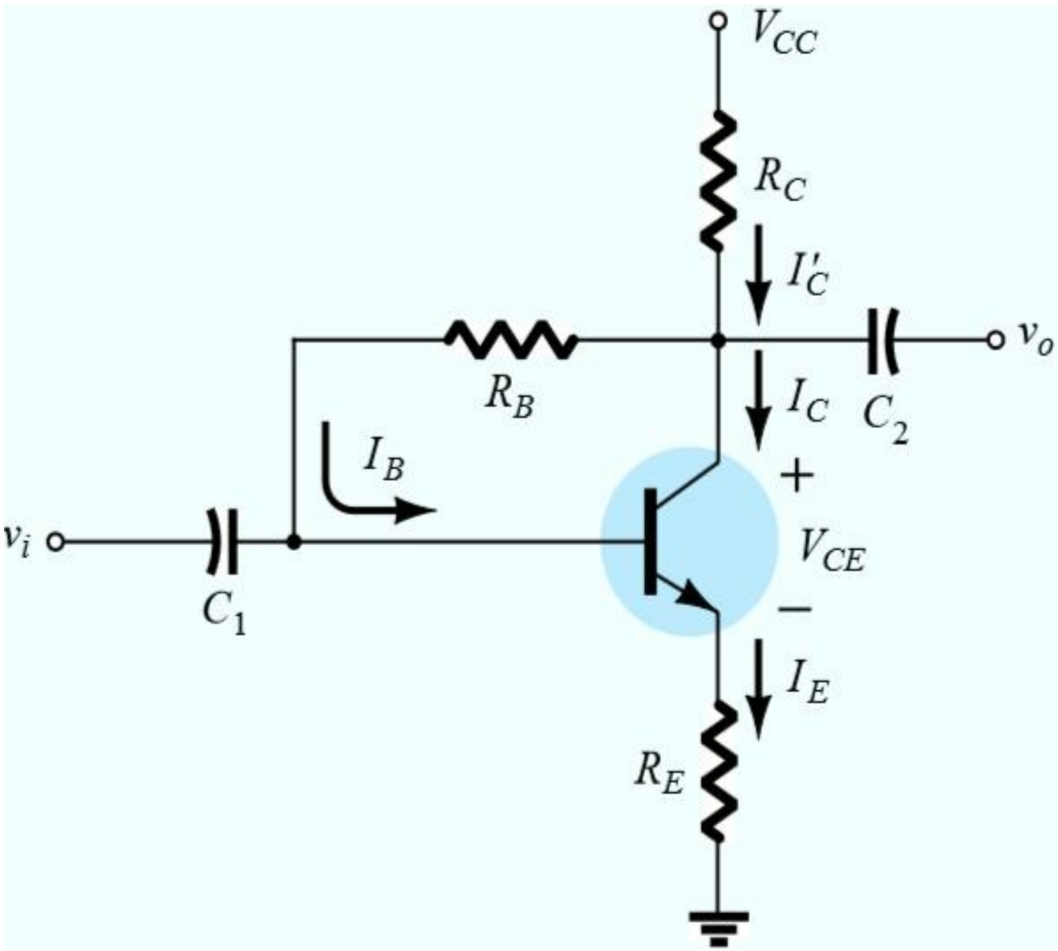
Voltage Divider Bias Circuit

Example:

Determine the dc bias voltage V_{CE} and the current I_C for the voltage divider configuration using exact analysis & approximate analysis.



DC Bias with Voltage Feedback:



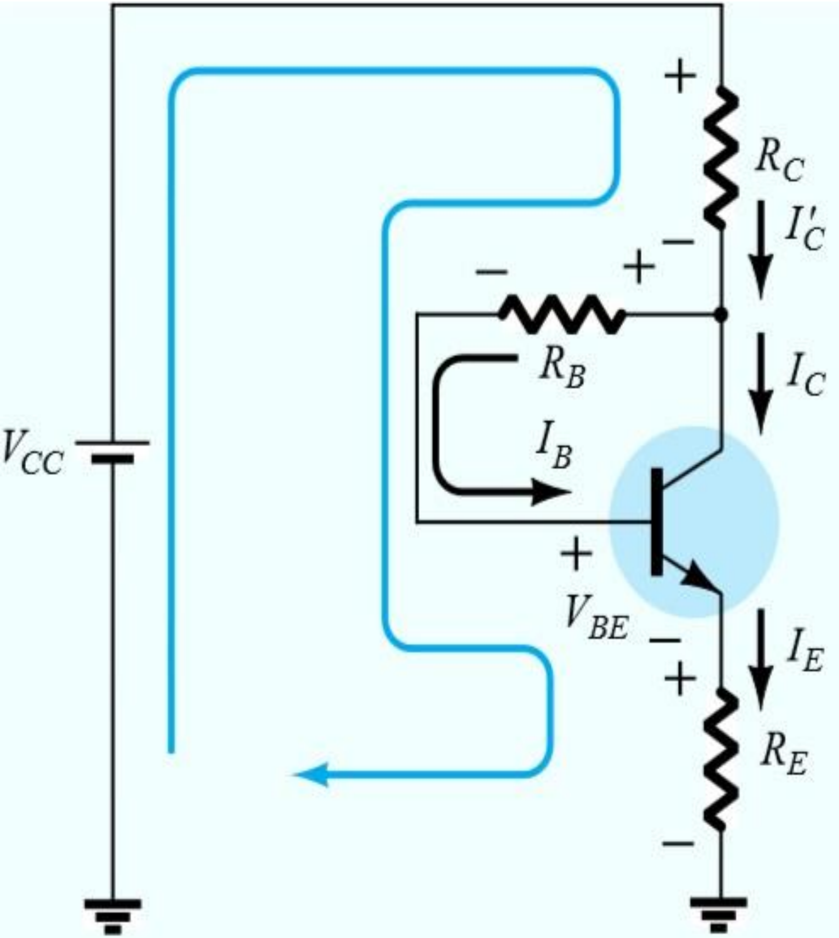
Here $I_C' = I_B + I_C$

The actual value of I_C & I_C' far exceeds the value of I_B.

Hence we can say that,

$$I'_C \approx I_C$$

DC Bias with Voltage Feedback:



Applying KVL in BE loop,

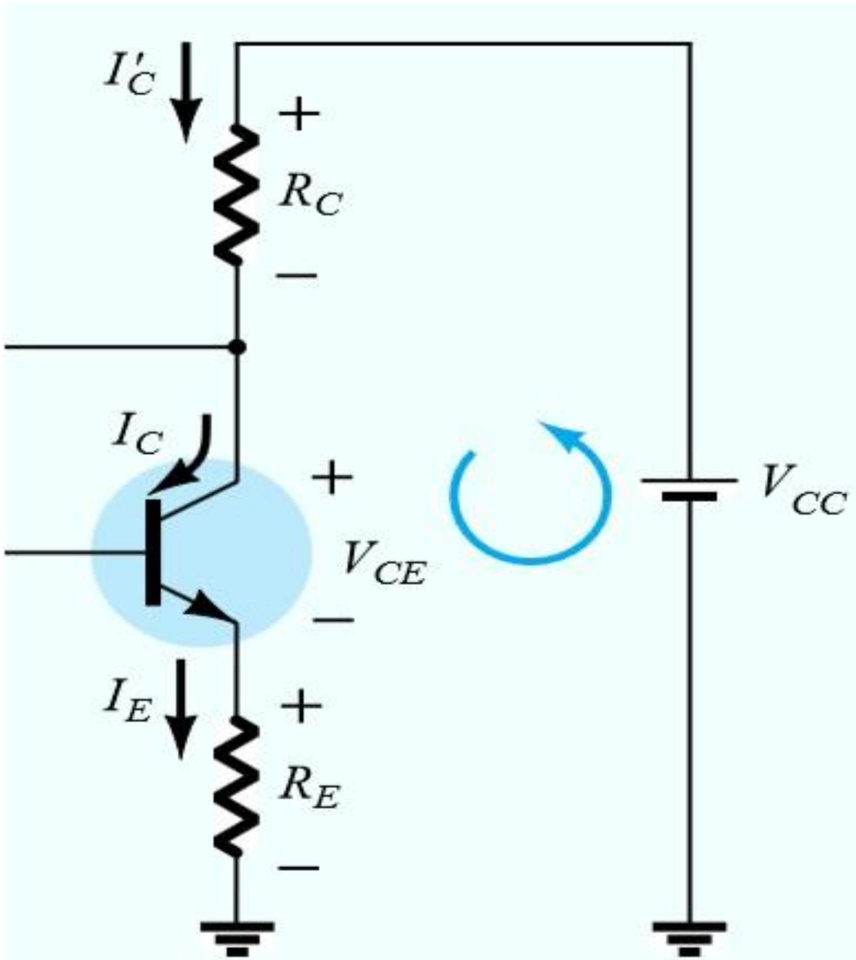
$V_{CC} - I'_C R_C - I_B R_B - V_{BE} - I_E R_E = 0$

$\Rightarrow V_{CC} - I_C R_C - I_B R_B - V_{BE} - I_E R_E = 0$

$\Rightarrow V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - (\beta+1) I_B R_E = 0$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_C + (\beta+1) R_E}$$

DC Bias with Voltage Feedback:



Applying KVL in CE loop,

$V_{CC} - I'_C R_C - V_{CE} - I_E R_E = 0$

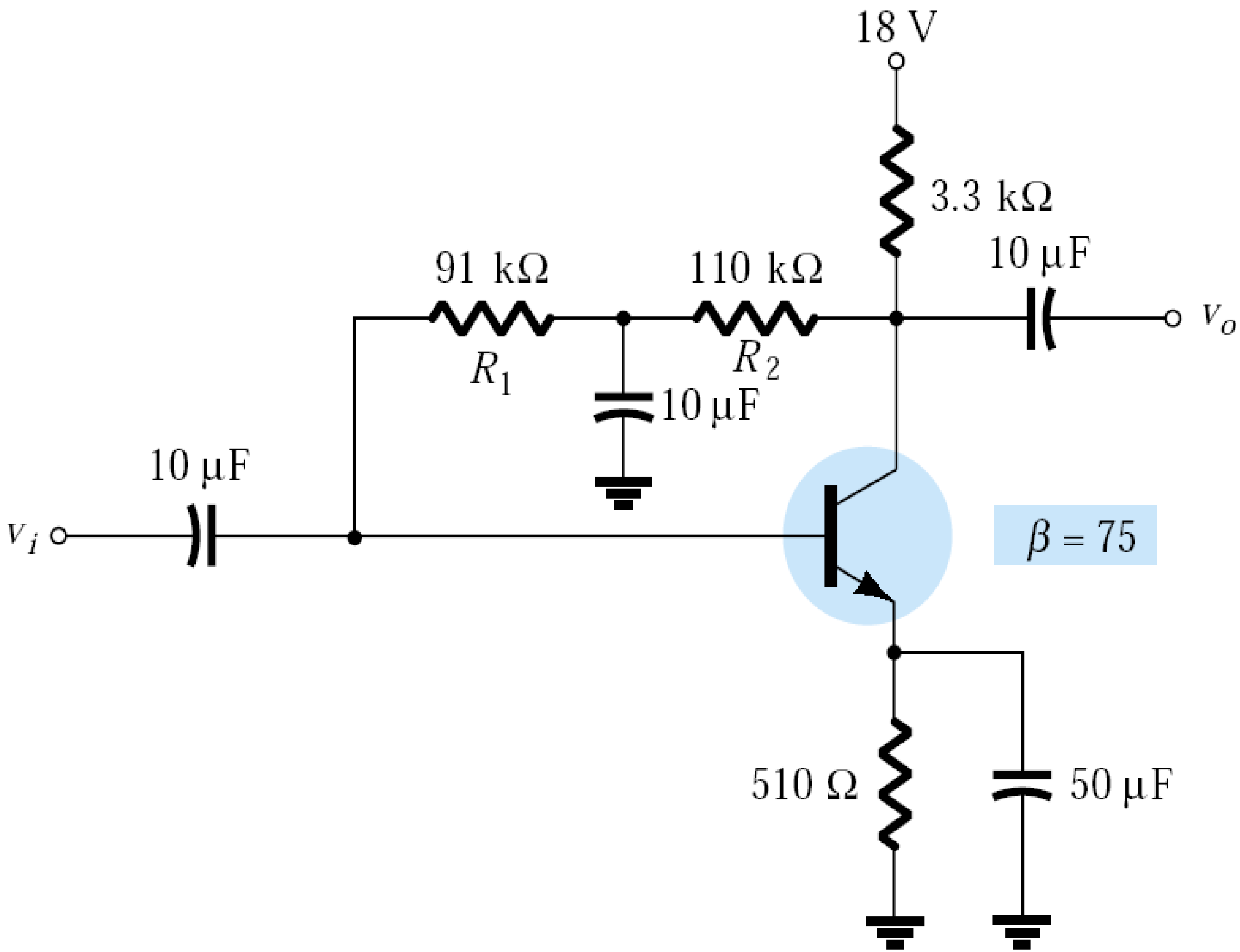
$\Rightarrow V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$

$\Rightarrow V_{CC} - I_C R_C - V_{CE} - I_C R_E = 0$

$\Rightarrow V_{CE} = V_{CC} - I_C (R_C + R_E)$

PRACTICE

DC Bias with Voltage Feedback:



Determine:

a) I_B

b) I_C

c) V_{CE}

d) V_E

e) V_C